CS-03-054

March 22, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/763,305 01/23/04

Jin Ping Liu et al.

METHOD OF FORMING A RELAXED SEMI-CONDUCTOR BUFFER LAYER ON A SUBSTRATE WITH A LARGE LATTICE MISMATCH

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 25, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 3/25/04

The following three U.S. Patents describe a graded SiGe buffer layer to spread lattice mimatch over a distance to minimize dislocations reaching the surface of the layer:

1) U.S. Patent 6,649,480 to Fitzgerald et al., "Method of Fabricating CMOS Inverter and Integrated Circuits Utilizing Strained Silicon Surface Channel MOSFETs."
2) U.S. Patent 6,583,015 to Fitzgerald et al., "Gate Technology for Strained Surface Channel and Strained Buried Channel MOSFET Devices."
3) U.S. Patent 6,646,322 to Fitzgerald, "Relaxed Silicon Germanium Platform for High Speed CMOS Electronics and High Speed Analog Circuits."

The following four U.S. Patents all disclose graded SiGe layers:

1) U.S. Patent 6,573,126 to Cheng et al., "Process for Producing Semiconductor Article Using Graded Epitaxial Growth."
2) U.S. Patent 6,515,335 to Christiansen et al., "Method for Fabrication of Relaxed Sige Buffer Layers on Silicon-On-Insulators and Structures Containing the Same."
3) U.S. Patent 5,859,864 to Jewell, "Extended Wavelength Lasers having a Restricted Growth Surface and Graded Lattice Mismatch."

4) U.S. Patent 5,821,577 to Crabbe' et al., "Graded Channel Field Effect Transistor."

U.S. Patent 6,649,492 to Chu et al., "Strained Si Based Layer Made by UHV-CVD, and Devices Therein," discloses varying Ge concentration in a SiGe layer.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Sheet 1 of 1

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
CS-03-054	10/763,305
Applicant: Jin Ping Liu et al.	
Filing Date: 01/23/04	Group Art Unit

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	6644632	11/11/03	Fitzgerald	257	531	7/16/01
	6649492	11/18/03	Chu et al.	438	478	2/11/02
	6649480	11/18/03	Fitzgerald et al.	438	285	6/19/01
	6583015	6/24/03	Fitzgerald et al.	438	287	8/6/01
	6573126	6/3/03	Cheng et al.	438	149	8/10/01
	6515335	2/4/03	Christiansen et al.	257	347	1/4/02
	5859864	1/12/99	Jewell	372	45	10/28/96
	5821577	10/13/98	Crabbé et al.	257	288	11/30/92

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant